UNIVERSAL CLOCK GENERATOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a clock generator, particularly to a universal clock generator suitable to be placed on every motherboard.

2. Description of Related Art

For the demands of different chipsets and personal computers, it is necessary to modify the structure of a clock generator. The output structure of a known clock generator 11 is shown in FIG. 1(a), which outputs clocks with all possible frequencies to all components (such as chipset 12 and DRAM module 13) on the motherboard. The output structure of another known clock generator 11 is shown in FIG. 1(b), which outputs a clock frequency to the chipset 12. After that, the chipset 12 outputs a reference frequency to a DRAM buffer 13, which further expands the number of clocks output to the DRAM module 13. Comparing to FIG. 1(a), it is more convenient to control the output of the DRAM frequency using the structure in FIG. 1(b). The output structure of a known clock generator 11 is shown in FIG. 1(c), which combines the DRAM buffer 14 and clock generator 11 in FIG. 1(b) into a single IC.

If the clock generator 11 is classified in accordance with the number of output clocks, it may be classified into a high frequency clock region 21 and a low frequency clock region 22, as shown in FIG. 2. The low frequency clock region 22 outputs fixed frequency clocks in general, such as 48/24 MHz, 14.318 MHz and the clock of an SM bus. Relatively, the design of a CPU clock, SDRAM clock, PCI clock and AGP clock in the high frequency clock region 21 always have to be modified according to the demand of the number of different clocks and the design of objects to which the clocks connect (such as a design of push and pull or open drain).

In other words, since the known clock generator 11 has to integrate different clock demands of different components on the motherboard, it will raise the manufacturing cost and lower down product compatibility due to a continuing modification. In order to solve with the above problem, the present invention proposes a novelty universal clock generator to overcome it.

SUMMARY OF THE INVENTION

The main object of the present invention is to provide a universal clock generator suitable to the demand of providing a large amount of different clock pins on a motherboard.

The second object of the present invention is to provide a universal clock generator so as to reduce the design and testing cost for motherboard and clock generator manufacturers.

To obtain the above purpose, the clock generator of the present invention comprises a high frequency clock region for generating high frequency clocks and a low frequency clock region for generating high frequency clocks. The low frequency clock region includes at least one delay lock loop for increasing the number of high frequency clocks of the high frequency clock region. When the number of the high frequency clocks (such as CPU clock, SDRAM clock, AGP clock and PCI clock) is not high enough, the delay lock loop of the low frequency clock region can be cascaded to support insufficient clocks. Besides, the output clocks of the delay lock loop can support a buffering function, and some clocks having a high variability (such as a CPU clock) can be set up as a push-pull, open-collector or differential output by a power-on setting pin for increasing the application.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be described according to the appended

drawings in which:

FIGS. 1(a) to (c) show prior art clock generators;

FIG. 2 shows a prior art clock generator; and

FIG. 3 shows a hint diagram of a universal clock generator of the present invention.

PREFERRED EMBODIMENT OF THE PRESENT INVENTION

FIG. 3 shows a hint diagram of a universal clock generator of the present invention, comprising a low frequency clock region 31, a high frequency clock region 32 and an oscillator 35 connecting to the low frequency clock region 31. The high frequency clock region 32 and low frequency clock region 31 can be grouped into a single chip or separated into two individual ICs. The low frequency clock region 31 includes a phase Lock Loop (PLL) connected to the oscillator 35 for generating prior 24/48/24.576 MHz clocks and 14.318 MHz clock. The high frequency clock region 32 also includes a PLL 35, which utilizes an output baseband clock (such as 14.318 MHz) of the PLL 33 in the low frequency clock region 31 as an input reference clock for generating a CPU clock, SDRAM clock, AGP clock and PCI clock. One characteristic of the present invention is that the low frequency clock region 31 includes a Delay Lock Loop (DLL) 34, which provides the function of a zero-delay clock buffering for duplicating necessary clocks. Therefore, the SDRAM clocks of the high frequency clock region 32 can connect to input ends of the DLL 34 of the low frequency clock region 31 so as to satisfy the demand of placing a large amount of different clock pins on a motherboard. Besides, output ends of the DLL 34 can also connect to input ends of the DLL for further increasing the number of output clocks. Furthermore, the low frequency clock region can further include at least one DLL 34 for increasing a usage complexity. In other words, the universal clock generator can meet the requirement of being adaptable to different designs

of motherboards, and a user merely needs to adjust the configuration of the DLL 34 of the low frequency clock region 31 to obtain the necessary number of clocks. In another aspect, since the present invention standardizes the clock generator, it facilitates the design a motherboard.

In addition, the output clocks of the DLL can support a buffering function, and some clocks having a high variability (such as a CPU clock) can be set up as a push-pull, open-collector or differential output by a power-on setting pin for increasing an application complexity.

The above-described embodiments of the present invention are intended to be illustrative only. Numerous alternative embodiments may be devised by those skilled in the art without departing from the scope of the following claims.